



Problems with Signal Integrity fall into 3 categories

1. Timing (not discussed but things in 1 clk cycle like gate flips etc)
2. Noise (this is a broad topic related to electrical properties of interconnects and how they impact waveforms)
3. Electromagnetic interference (EMI)

Noise: Lots of different noise problems exists with signal integrity: ringing ground bounce cross talk etc. These problems arise from electrical properties of interconnects and how these properties affect waveforms of high speed interconnects

There may be a ton of names for noise related issues but they all relate to 1 of 4 core problems

1. Signal quality of one net incl losses on the line
2. Cross talk between two or more nets incl gnd + pow balance
3. Rail collapse in the power + gnd distribution
4. Electromagnetic interference and radiation from the entire system

If we understand the principles behind these 4 noises the solutions become obvious very powerful to classify all problems to this

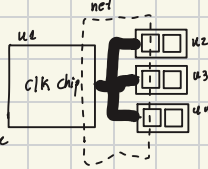
Signal quality of a net...

What is a net? just metal connected together in a system

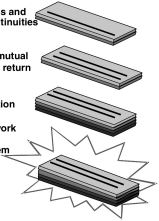
ex. trace from clk chip output pin to thumb chips

↳ Nets aren't just the signal path but also the return path for signal current

Signal quality for singular nets depend on physical features of the trace as on the return path



1. Signal quality of one net: reflections and distortions from impedance discontinuities in the signal or return path
2. Cross talk between multiple nets: mutual C and mutual L coupling with ideal return paths and non-ideal return paths
3. Rail collapse in the power distribution system (PDS): voltage drop across the impedance in the power network
4. EMI from a component or the system



Include a terms list for anything to say resistance = impedance is a gross simplification

When signals leave the output the signal (made up of V and I)

see the connection time as impedance as signals propagate down the net it checks the instantaneous impedance. If it stays constant the signal is undistorted if it does defect change signal distortion reflect propagate

↳ terrible if this too many changes false triggering can occur

Okay so what affects impedance

features which change the cross section or geometric shape of net

→ feats. which change the impedance are a discontinuity each one causes distortion

1. line width change
2. layer change through a via
3. traps in return plane paths
4. connectors
5. branch tee stub
6. End of net

Discontinuities can come from cross section topology of routed traces or components

↳ commonly happens at the ends of traces

To minimize problems with impedance you want to keep the impedance the signal sees constant through the net

Ways to keep impedance constant for said signals

1. Board with constant / controlled impedance traces

• uniform transmission lines

2. Routing rules which allow topology to maintain constant impedance down a trace

3. Strategic resistors to manipulate reflections keep things clean

↳ terminating resistors can be used to manage impedance changes in the same net

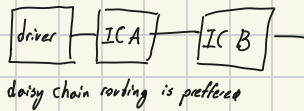
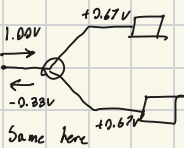
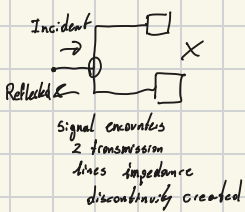
↳ "ringing" largely is just reflections due to impedance changes

Terminations can only go so far precise board layout also plays a role

Traces which branch into 2 paths

→ Impedance at the junction changes and a portion of the signal reflects back while some continues down the branch

↳ Routing daisy chain wire signal sees constant impedance all down the path



$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad Z_{\text{junction}} = 50 // 50 = 25 \Omega$$
$$\frac{25 - 50}{25 + 50} = -\frac{1}{3}$$

$$V_{\text{transmitted}} = V_{\text{incident}} (1 + \Gamma)$$

The impact of said discontinuity depends on the rise time of the signal sholder = greater signal distortion

Try to keep impedance constant always (method which achieves this is using controlled impedance interconnects etc.)

Aside from changes in impedance there are 2 other ways signal quality is affected

1. Frequency dependent losses of the conductor + dielectric causes high freq components to be attenuated more than lower ones

↳ Increases the rise time when this approaches the period of a bit the info is distorted

concept is known as inter symbol interference (ISI)

2. Timing specifically time delay differences between 2 or more paths is called **Skew** if signal and clk have skew false triggering can happen. If skew is in a differential pair the differential signal will be distorted (ISI + false triggers)

Skew is fundamentally a timing issue it arises due to properties of the interconnect

→ The total length of interconnects matter keep differential pairs same length

→ Can be related to local dielectric constant each signal sees (more difficult)

Cross talk

→ When a net carries a signal some of the current/voltage passes over to an adjacent net minding it's own business
↳ signal quality of active net may be perfect but some signal can appear as unwanted noise on other net

It comes from capacitive + inductive coupling between 2 nets providing path for unwanted noise between them

Occurs in 2 different environments

1. When interconnects are uniform transmission lines
2. When they aren't (connectors/packages)

controlled Impedance lines with wide uniform return paths amount of capacitive + inductive coupling is comparable

The 2 effects combine in separate ways at near ends of a quiet line and far end

A wide uniform return plane is the configuration with lowest cross talk

↳ Anything that changes the return path from a wide uniform plane will increase coupled noise between lines

When inductively coupled noise dominates the cross talk is referred to as switching noise / ground bounce / simultaneous switching noise SSN
this noise is generated by coupled inductance (mutual inductance) and happens mostly in connectors vias packages places where return path isn't a uniform plane

understanding the nature of capacitive / inductive coupling allows us to possibly optimize the physical design of adjacent signal traces to minimize coupling. Spacing lines apart, using lower dielectric constant material and even increasing length + decreasing the rise times. keep interconnects short using CSPs and high density interconnects minimize

Rail collapse noise

→ Noise is generated this is a problem not in only signal paths but can mess up power and ground distribution networks which lead the chip

When current through power + gnd path change there's a voltage drop across the impedance of power gnd paths. The drop means less voltage gets to the chip → decrease or collapse of voltage between power + gnd rails

The goal in designing power + gnd distribution is to try and minimize the impedance of the power distribution system/networks

1. closely spaced adjacent planes for power + gnd distribution with a thin dielectric between them near the surface
2. multiple low inductance decoupling capacitors
3. multiple very short power and ground leads
4. on chip decoupling capacitance

Electromagnetic Interference

→ When we introduce boards with clock frequencies in 100 - 500 MHz range the first few harmonics are within communication bands of TV radio phones
now there exists a real possibility that electronic products can interfere with communications unless EMI is kept at acceptable levels

It takes 3 things to have an EMI problem

- source of noise
- pathway to radiator
- Antenna

The 2 most common sources of EMI are

1. The conversion of some differential signal to common signal
2. ground bounce on a circuit board generating common currents on external single shielded cables

You can isolate it by grouping highspeed sections of board away from where the exit

↳ Shielding boxes can also help